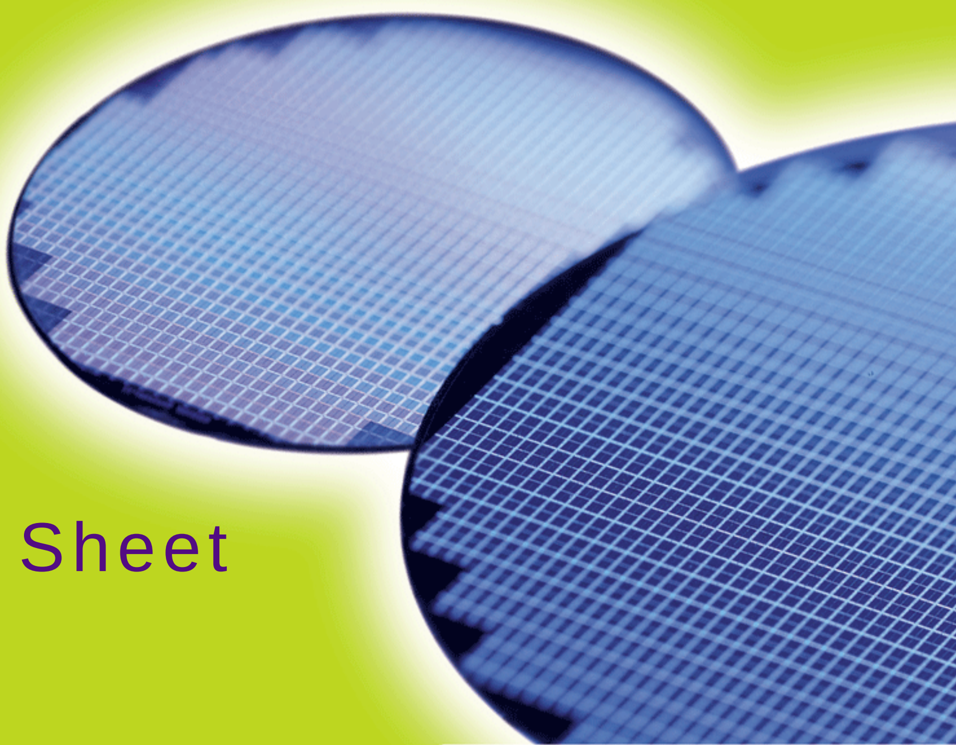
June 2008

HYS64T512020EU–[25F/2.5/3S]–A
HYS72T512020EU–[25F/2.5/3S]–A

240-Pin Unbuffered DDR2 SDRAM Modules
UDIMM SDRAM
EU RoHS Compliant



Internet Data Sheet

Rev. 1.0

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HYS64T512020EU–[25F/2.5/3S]–A, HYS72T512020EU–[25F/2.5/3S]–A Internet Data Sheet Revision History: 2008-06, Rev. 1.0	
Page	**Subjects (major changes since last revision)**
All	Removed HYS[64/72]T512020EU-[3/3.7]-A product types and added Idd values and adapted to internet edition.
Previous Revision: Rev. 0.20, 2007-07	
All	Datasheet for HYS[64/72]T512020EU-[25F/2.5/3/3S/3.7]-A.

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1 Overview

This chapter gives an overview of the 240-pin Unbuffered DDR2 SDRAM modules product family and describes its main characteristics.

1.1 Features

- 240-Pin PC2-6400 and PC2-5300 DDR2 SDRAM memory modules.
- Two ranks 512M × 64, 512M × 72 module organization, and 256M × 8 chip organization.
- 4GB Modules built with 2 Gbit DDR2 SDRAMs in chipsize packages PG-TFBGA-68.
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply.
- All speed grades faster than DDR2-400 comply with DDR2-400 timing specifications.
- Programmable CAS Latencies (3, 4, 5, 6 and 7), Burst Length (8 & 4).
- Auto Refresh (CBR) and Self Refresh.
- Auto Refresh for temperatures above 85 °C t_{REFI} = 3.9 µs.
- Programmable self refresh rate via EMRS2 setting.
- Programmable partial array refresh via EMRS2 settings.
- DCC enabling via EMRS2 setting.
- All inputs and outputs SSTL_1.8 compatible.
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT).
- Serial Presence Detect with E^{2}PROM.
- UDIMM and EDIMM Dimensions (nominal): 30 mm high, 133.35 mm wide
- Based on standard reference layouts Raw Cards 'E' and 'G'.
- RoHS compliant products[1].

TABLE 1
Performance Table

QAG Speed Code			**–25F**	**–2.5**	**–3S**	**Unit**	**Note**
DRAM Speed Grade		**DDR2**	**–800D**	**–800E**	**–667D**	t_{CK}	
Module Speed Grade		**PC2**	**–6400D**	**–6400E**	**–5300D**		
CAS-RCD-RP latencies			**5–5–5**	**6–6–6**	**5–5–5**		
Max. Clock Frequency	CL3	f_{CK3}	200	200	200	MHz	
	CL4	f_{CK4}	266	266	266	MHz	
	CL5	f_{CK5}	400	333	333	MHz	
	CL6	f_{CK6}	–	400	–	MHz	
Min. RAS-CAS-Delay		t_{RCD}	12.5	15	15	ns	
Min. Row Precharge Time		t_{RP}	12.5	15	15	ns	
Min. Row Active Time		t_{RAS}	45	45	45	ns	
Min. Row Cycle Time		t_{RC}	57.5	60	60	ns	
Precharge-All (8 banks) command period		t_{PREA}	15	17.5	18	ns	1)2)

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers. For more information please visit **www.qimonda.com/green_products** .

1) This t_{PREA} value is the minimum value at which this chip will be functional.
2) Precharge-All command for an 8 bank device will equal to t_{RP} + 1 × t_{CK} or t_{nRP} + 1 × nCK, depending on the speed bin, where t_{nRP} = RU{ t_{RP} / $t_{CK(avg)}$ } and t_{RP} is the value for a single bank precharge.

1.2 Description

The Qimonda HYS[64/72]T512020EU–[25F/2.5/3S]–A module family are Unbuffered DIMM modules "UDIMMs" with 30 mm height based on DDR2 technology. DIMMs are available as non-ECC modules in 512M × 64 (4GB) and as ECC modules in 512M × 72 (4GB) in organization and density, intended for mounting into 240-pin connector sockets.

The memory array is designed with 2 Gbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.

green Product

TABLE 2
Ordering Information

Product Type[1)]	Compliance Code[2)]	Description	SDRAM Technology
PC2-6400 (5-5-5)			
HYS64T512020EU-25F-A	4GB 2R×8 PC2–6400U–555–12–E0	2 Ranks, Non-ECC	2Gbit (×8)
HYS72T512020EU-25F-A	4GB 2R×8 PC2–6400E–555–12–G0	2 Ranks, ECC	2Gbit (×8)
PC2-6400 (6-6-6)			
HYS64T512020EU-2.5-A	4GB 2R×8 PC2–6400U–666–12–E0	2 Ranks, Non-ECC	2Gbit (×8)
HYS72T512020EU-2.5-A	4GB 2R×8 PC2–6400E–666–12–G0	2 Ranks, ECC	2Gbit (×8)
PC2-5300 (5-5-5)			
HYS64T512020EU-3S-A	4GB 2R×8 PC2–5300U–555–12–E0	2 Ranks, Non-ECC	2Gbit (×8)
HYS72T512020EU-3S-A	4GB 2R×8 PC2–5300E–555–12–G0	2 Ranks, ECC	2Gbit (×8)

1) For detailed information regarding Product Type of Qimonda please see chapter "Product Type Nomenclature" of this data sheet.
2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC2–6400E–555–12–G0" where 6400E means Unbuffered DIMM modules with 6.40 GB/sec Module Bandwidth and "555–12" means Column Address Strobe (CAS) latency =5, Row Column Delay (RCD) latency = 5 and Row Precharge (RP) latency = 5 using the Industry Standard SPD Revision 1.2 and produced on the Raw Card "G".

TABLE 3
Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/column bits	Raw Card
4GB	512M × 64	2	Non-ECC	16	15/3/10	E
4GB	512M × 72	2	ECC	18	15/3/10	G

TABLE 4
Components on Modules

Product Type[1)2)]	DRAM Components[1)]	DRAM Density	DRAM Organisation
HYS64T512020EU	HYB18T2G800AF	2Gbit	256M × 8
HYS72T512020EU	HYB18T2G800AF	2Gbit	256M × 8

1) Green Product
2) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

2 Pin Configurations and Block Diagrams

2.1 Pin Configurations

The pin configuration of the Unbuffered DDR2 SDRAM DIMM is listed by function in **Table 5** (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 6** and **Table 7** respectively. The pin numbering is depicted in **Figure 1** for non-ECC modules (×64) and **Figure 2** for ECC modules (×72).

TABLE 5
Pin Configuration of UDIMM

Ball No.	Name	Pin Type	Buffer Type	Function
Clock Signals				
185	CK0	I	SSTL	**Clock Signals 2:0, Complement Clock Signals 2:0** The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{\text{CK}}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
137	CK1	I	SSTL	
220	CK2	I	SSTL	
186	$\overline{\text{CK0}}$	I	SSTL	
138	$\overline{\text{CK1}}$	I	SSTL	
221	$\overline{\text{CK2}}$	I	SSTL	
52	CKE0	I	SSTL	**Clock Enable Rank 1:0** Activates the DDR2 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE LOW initiates the Power Down Mode or the Self Refresh Mode. *Note: 2 Ranks module*
171	CKE1	I	SSTL	
	NC	NC	—	**Not Connected** *Note: 1 Rank module*
Control Signals				
193	$\overline{\text{S0}}$	I	SSTL	**Chip Select Rank 1:0** Enables the associated DDR2 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{\text{S0}}$; Rank 1 is selected by $\overline{\text{S1}}$. Ranks are also called "Physical banks". *Note: 2 Ranks module*
76	$\overline{\text{S1}}$	I	SSTL	
	NC	NC	—	**Not Connected** *Note: 1 Rank module*
192	$\overline{\text{RAS}}$	I	SSTL	**Row Address Strobe** When sampled at the cross point of the rising edge of CK,and falling edge of $\overline{\text{CK}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ define the operation to be executed by the SDRAM.
74	$\overline{\text{CAS}}$	I	SSTL	**Column Address Strobe**

Ball No.	Name	Pin Type	Buffer Type	Function
73	$\overline{\text{WE}}$	I	SSTL	**Write Enable**
Address Signals				
71	BA0	I	SSTL	**Bank Address Bus 1:0** Selects which DDR2 SDRAM internal bank of four or eight is activated.
190	BA1	I	SSTL	
54	BA2	I	SSTL	**Bank Address Bus 2** Greater than 512Mb DDR2 SDRAMS
	NC	NC	—	**Not Connected** Less than 1Gb DDR2 SDRAMS
188	A0	I	SSTL	**Address Bus 12:0** During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{\text{CK}}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is LOW, then BA0-BAn are used to define which bank to precharge.
183	A1	I	SSTL	
63	A2	I	SSTL	
182	A3	I	SSTL	
61	A4	I	SSTL	
60	A5	I	SSTL	
180	A6	I	SSTL	
58	A7	I	SSTL	
179	A8	I	SSTL	
177	A9	I	SSTL	
70	A10	I	SSTL	
	AP	I	SSTL	
57	A11	I	SSTL	
176	A12	I	SSTL	
196	A13	I	SSTL	**Address Signal 13** *Note: 1 Gbit based module and 512M ×4/×8*
	NC	NC	—	**Not Connected** *Note: Module based on 1 Gbit ×16Module based on 512 Mbit ×16 or smaller*
174	A14	I	SSTL	**Address Signal 14** *Note: Modules based on 2 Gbit*
	NC	NC	—	**Not Connected** *Note: Modules based on 1 Gbit or smaller*
Data Signals				
3	DQ0	I/O	SSTL	**Data Bus 63:0** Data Input / Output pins
4	DQ1	I/O	SSTL	
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
122	DQ4	I/O	SSTL	
123	DQ5	I/O	SSTL	
128	DQ6	I/O	SSTL	
129	DQ7	I/O	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
12	DQ8	I/O	SSTL	**Data Bus 63:0** Data Input / Output pins
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
131	DQ12	I/O	SSTL	
132	DQ13	I/O	SSTL	
140	DQ14	I/O	SSTL	
141	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
143	DQ20	I/O	SSTL	
144	DQ21	I/O	SSTL	
149	DQ22	I/O	SSTL	
150	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
152	DQ28	I/O	SSTL	
153	DQ29	I/O	SSTL	
158	DQ30	I/O	SSTL	
159	DQ31	I/O	SSTL	
80	DQ32	I/O	SSTL	
81	DQ33	I/O	SSTL	
86	DQ34	I/O	SSTL	
87	DQ35	I/O	SSTL	
199	DQ36	I/O	SSTL	
200	DQ37	I/O	SSTL	
205	DQ38	I/O	SSTL	
206	DQ39	I/O	SSTL	
89	DQ40	I/O	SSTL	
90	DQ41	I/O	SSTL	
95	DQ42	I/O	SSTL	
96	DQ43	I/O	SSTL	
208	DQ44	I/O	SSTL	
209	DQ45	I/O	SSTL	
214	DQ46	I/O	SSTL	
215	DQ47	I/O	SSTL	

Ball No.	Name	Pin Type	Buffer Type	Function
98	DQ48	I/O	SSTL	**Data Bus 63:0** Data Input / Output pins
99	DQ49	I/O	SSTL	
107	DQ50	I/O	SSTL	
108	DQ51	I/O	SSTL	
217	DQ52	I/O	SSTL	
218	DQ53	I/O	SSTL	
226	DQ54	I/O	SSTL	
227	DQ55	I/O	SSTL	
110	DQ56	I/O	SSTL	
111	DQ57	I/O	SSTL	
116	DQ58	I/O	SSTL	
117	DQ59	I/O	SSTL	
229	DQ60	I/O	SSTL	
230	DQ61	I/O	SSTL	
235	DQ62	I/O	SSTL	
236	DQ63	I/O	SSTL	
Check Bit Signals				
42	CB0	I/O	SSTL	**Check Bit 0** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: Non-ECC type module only*
43	CB1	I/O	SSTL	**Check Bit 1** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: Non-ECC type module only*
48	CB2	I/O	SSTL	**Check Bit 2** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: Non-ECC type module only*
49	CB3	I/O	SSTL	**Check Bit 3** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: Non-ECC type module only*
161	CB4	I/O	SSTL	**Check Bit 4** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: Non-ECC type module only*
162	CB5	I/O	SSTL	**Check Bit 5** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: Non-ECC type module only*

Ball No.	Name	Pin Type	Buffer Type	Function
167	CB6	I/O	SSTL	**Check Bit 6** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: Non-ECC type module only*
168	CB7	I/O	SSTL	**Check Bit 7** *Note: ECC type module only*
	NC	NC	—	**Not Connected** *Note: Non-ECC module only*
Data Strobe Bus				
7	DQS0	I/O	SSTL	**Data Strobe Bus 8:0** The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. $\overline{\text{DQS}}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{\text{DQS}}$. If the module is to be operated in single ended strobe mode, all $\overline{\text{DQS}}$ signals must be tied on the system board to V_{SS} and DDR2 SDRAM mode registers programmed appropriately.
16	DQS1	I/O	SSTL	
28	DQS2	I/O	SSTL	
37	DQS3	I/O	SSTL	
84	DQS4	I/O	SSTL	
93	DQS5	I/O	SSTL	
105	DQS6	I/O	SSTL	
114	DQS7	I/O	SSTL	
46	DQS8	I/O	SSTL	
6	$\overline{\text{DQS0}}$	I/O	SSTL	**Complement Data Strobe Bus 8:0**
15	$\overline{\text{DQS1}}$	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
36	$\overline{\text{DQS3}}$	I/O	SSTL	
83	$\overline{\text{DQS4}}$	I/O	SSTL	
92	$\overline{\text{DQS5}}$	I/O	SSTL	
104	$\overline{\text{DQS6}}$	I/O	SSTL	
113	$\overline{\text{DQS7}}$	I/O	SSTL	
45	$\overline{\text{DQS8}}$	I/O	SSTL	
Data Mask Signals				
125	DM0	I	SSTL	**Data Mask Bus 8:0** The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect.
134	DM1	I	SSTL	
146	DM2	I	SSTL	
155	DM3	I	SSTL	
202	DM4	I	SSTL	
211	DM5	I	SSTL	
223	DM6	I	SSTL	
232	DM7	I	SSTL	
164	DM8	I	SSTL	
EEPROM				
120	SCL	I	CMOS	**Serial Bus Clock** This signal is used to clock data into and out of the SPD EEPROM.

Ball No.	Name	Pin Type	Buffer Type	Function
119	SDA	I/O	OD	**Serial Bus Data** This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to V_{DDSPD} on the motherboard to act as a pull-up.
239	SA0	I	CMOS	**Serial Address Select Bus 2:0** Address pins used to select the Serial Presence Detect base address.
240	SA1	I	CMOS	
101	SA2	I	CMOS	
Power Supplies				
1	V_{REF}	AI	—	**I/O Reference Voltage** Reference voltage for the SSTL-18 inputs.
238	V_{DDSPD}	PWR	—	**EEPROM Power Supply** Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
51,56,62,72,75,, 78,170,175,181,, 191,194	V_{DDQ}	PWR	—	**I/O Driver Power Supply**
53,59,64,67,69,, 172,178,184,187, 189,197	V_{DD}	PWR	—	**Power Supply** Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
2,5,8,11,14,17,, 20,23,26,29,32, 35,38,41,44,47,, 50,65,66,79,82, 85,88,91,94,97,, 100,103,106, 109,112,115,118, 121,124,127,, 130,133,136,139, 142,145,148,, 151,154,157,160, 163,166,169, 198,201,204,207, 210,213,216,, 219,222,225,228, 231,234,237	V_{SS}	GND	—	**Ground Plane** Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
Other Pins				
195	ODT0	I	SSTL	**On-Die Termination Control 0**
77	ODT1	I	SSTL	**On-Die Termination Control 1** Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ signals if enabled via the DDR2 SDRAM mode register. *Note: 2 Rank modules*
	NC	NC	—	**Not Connected** *Note: 1 Rank modules*
18,19,55,68,102,1 26,135,147, 156,165,173,203, 212, 224,233	NC	NC	—	**Not connected** *Note: Pins not connected on Qimonda UDIMMs*

TABLE 6
Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 7
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tri-state, and allows multiple devices to share as a wire-OR.

FIGURE 1
Pin Configuration UDIMM ×72 (240 Pin)

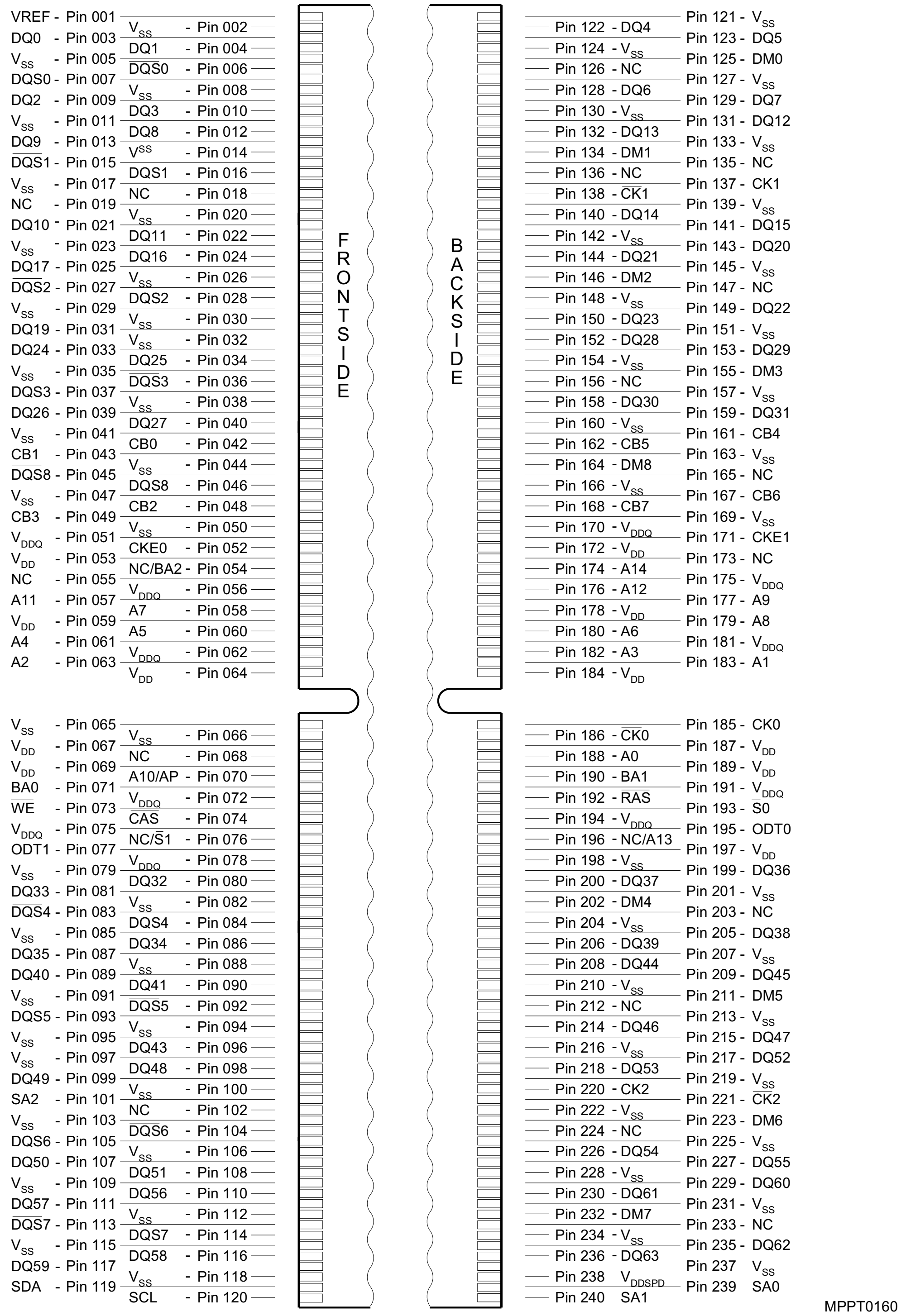
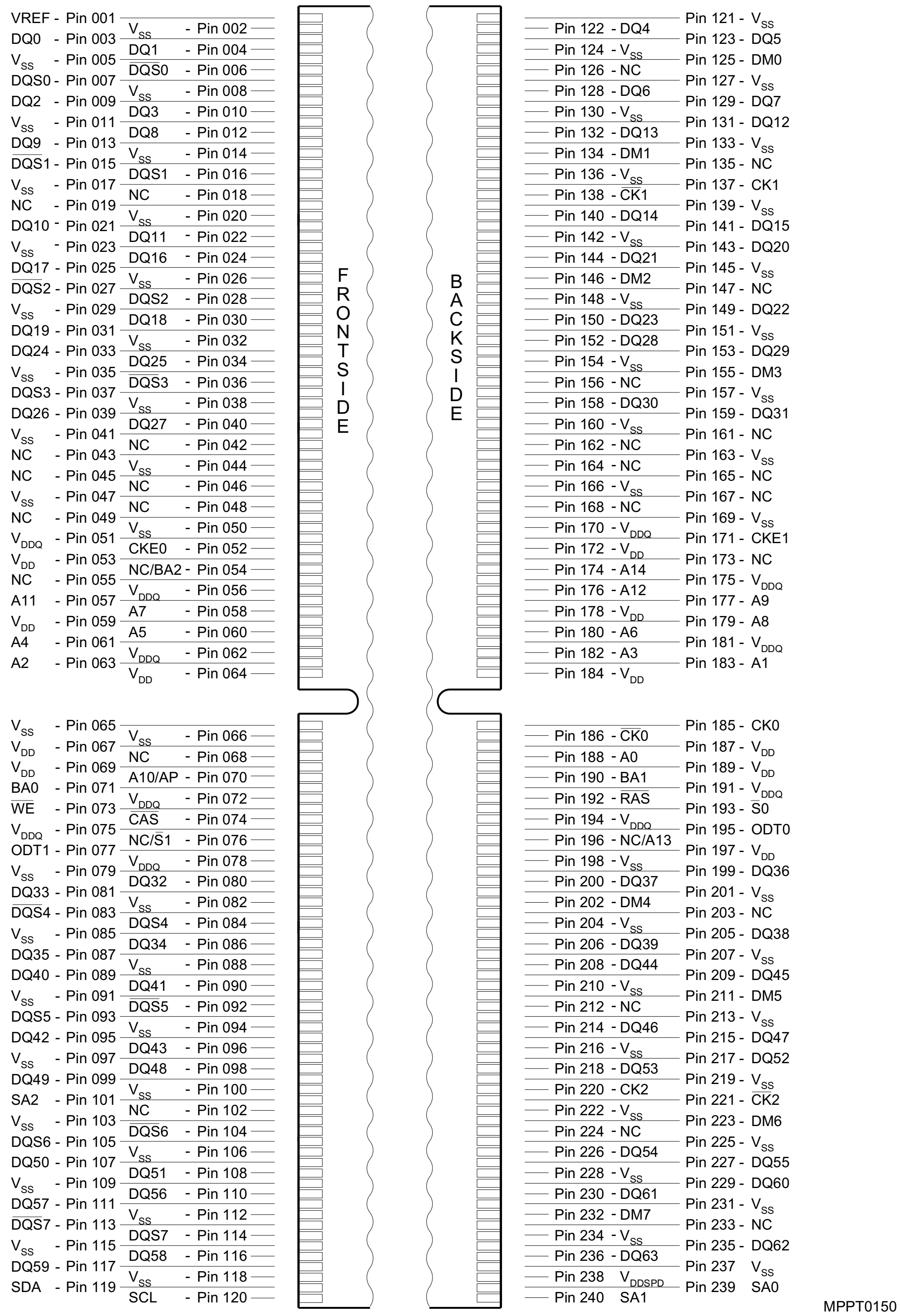


FIGURE 2
Pin Configuration UDIMM ×64 (240 Pin)



3 Electrical Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

3.1 Absolute Maximum Ratings

***Attention:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

TABLE 8
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–1.0	+2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.5	+2.3	V	
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	–0.5	+2.3	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.5	+2.3	V	

1) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.

TABLE 9
Environmental Requirements

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	0	+55	°C	1)
Storage Temperature	T_{STG}	– 50	+100	°C	2)
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	3)
Operating Humidity (relative)	H_{OPR}	10	90	%	
Storage Humidity (without condensation)	H_{STG}	5	95	%	

1) The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR2 DRAM component specification.
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3) Up to 3000 m.

TABLE 10
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{CASE}	Operating Temperature	0	95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3) Above 85 °C the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs
4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%

3.2 DC Operating Conditions

TABLE 11
Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	
DC Input Logic High	$V_{IH(DC)}$	V_{REF} + 0.125	—	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	—	V_{REF} – 0.125	V	
In / Output Leakage Current	I_L	– 5	—	5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC).V_{REF} is also expected to track noise in V_{DDQ}.
3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin

3.3 Speed Grade Definitions

TABLE 12
Speed Grade Definition

Speed Grade			DDR2–800D		DDR2–800E		Unit	Note
QAG Sort Name			–25F		–2.5			
CAS-RCD-RP latencies			5–5–5		6–6–6		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Period	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	2.5	8	3	8	ns	1)2)3)4)
	@ CL = 6	t_{CK}	2.5	8	2.5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70k	45	70k	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	57.5	—	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	12.5	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	12.5	—	15	—	ns	1)2)3)4)

TABLE 13
Speed Grade Definition

Speed Grade			DDR2–667D		Unit	Note
QAG Sort Name			–3S			
CAS-RCD-RP latencies			5–5–5		t_{CK}	
Parameter		Symbol	Min.	Max.	—	
Clock Period	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70k	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{\text{CK}}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
2) The CK/$\overline{\text{CK}}$ input reference level (for timing reference to CK/$\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross. The DQS / $\overline{\text{DQS}}$, RDQS / $\overline{\text{RDQS}}$, input reference level is the crosspoint when in differential strobe mode.
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ}
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

3.4 Component AC Timing Parameters

TABLE 14
DRAM Component Timing Parameter by Speed Grade - DDR2–800 and DDR2–667

Parameter	Symbol	DDR2–800		DDR2–667		Unit	Note1)2)3)4)5)6)7)
		Min.	Max.	Min.	Max.		
CAS to CAS command delay	t_{CCD}	2	—	2	—	nCK	
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	0.48	0.52	$t_{CK.AVG}$	9)10)
Average clock period	$t_{CK.AVG}$	2500	8000	3000	8000	ps	
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	—	3	—	nCK	11)
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	0.48	0.52	$t_{CK.AVG}$	9)10)
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{nRP}	—	WR + t_{nRP}	—	nCK	12)13)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + $t_{CK.AVG}$ + t_{IH}	—	t_{IS} + $t_{CK.AVG}$ + t_{IH}	—	ns	
DQ and DM input hold time	$t_{DH.BASE}$	125	—	175	—	ps	14)18)19)
DQ and DM input pulse width for each input	t_{DIPW}	0.35	—	0.35	—	$t_{CK.AVG}$	
DQS input high pulse width	t_{DQSH}	0.35	—	0.35	—	$t_{CK.AVG}$	
DQS input low pulse width	t_{DQSL}	0.35	—	0.35	—	$t_{CK.AVG}$	
DQS-DQ skew for DQS & associated DQ signals	t_{DQSQ}	—	200	—	240	ps	15)
DQS latching rising transition to associated clock edges	t_{DQSS}	– 0.25	+ 0.25	– 0.25	+ 0.25	$t_{CK.AVG}$	16)
DQ and DM input setup time	$t_{DS.BASE}$	50	—	100	—	ps	17)18)19)
DQS falling edge hold time from CK	t_{DSH}	0.2	—	0.2	—	$t_{CK.AVG}$	16)
DQS falling edge to CK setup time	t_{DSS}	0.2	—	0.2	—	$t_{CK.AVG}$	16)
Four Activate Window for 1KB page size products	t_{FAW}	35	—	37.5	—	ns	34)
Four Activate Window for 2KB page size products	t_{FAW}	45	—	50	—	ns	34)
CK half pulse width	t_{HP}	Min($t_{CH.ABS}$, $t_{CL.ABS}$)	—	Min($t_{CH.ABS}$, $t_{CL.ABS}$)	—	ps	20)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	—	$t_{AC.MAX}$	ps	8)21)
Address and control input hold time	$t_{IH.BASE}$	250	—	275	—	ps	22)24)
Control & address input pulse width for each input	t_{IPW}	0.6	—	0.6	—	$t_{CK.AVG}$	
Address and control input setup time	$t_{IS.BASE}$	175	—	200	—	ps	23)24)
DQ low impedance time from CK/$\overline{CK}$	$t_{LZ.DQ}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	ps	8)21)

Parameter	Symbol	DDR2–800		DDR2–667		Unit	Note1)2)3)4)5)6)7)
		Min.	Max.	Min.	Max.		
DQS/$\overline{\text{DQS}}$ low-impedance time from CK / $\overline{\text{CK}}$	$t_{LZ.DQS}$	$t_{AC.MIN}$	$t_{AC.MAX}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	8)21)
MRS command to ODT update delay	t_{MOD}	0	12	0	12	ns	34)
Mode register set command cycle time	t_{MRD}	2	—	2	—	nCK	
OCD drive mode output delay	t_{OIT}	0	12	0	12	ns	34)
DQ/DQS output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—	ps	25)
DQ hold skew factor	t_{QHS}	—	300	—	340	ps	26)
Average periodic refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	27)28)
		—	3.9	—	3.9	µs	27)29)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	127.5	—	127.5	—	ns	30)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	$t_{CK.AVG}$	31)32)
Read postamble	t_{RPST}	0.4	0.6	0.4	0.6	$t_{CK.AVG}$	31)33)
Active to active command period for 1KB page size products	t_{RRD}	7.5	—	7.5	—	ns	34)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	7.5	—	ns	34)
Write preamble	t_{WPRE}	0.35	—	0.35	—	$t_{CK.AVG}$	
Write postamble	t_{WPST}	0.4	0.6	0.4	0.6	$t_{CK.AVG}$	
Write recovery time	t_{WR}	15	—	15	—	ns	34)
Internal write to read command delay	t_{WTR}	7.5	—	7.5	—	ns	34)35)
Exit power down to read command	t_{XARD}	2	—	2	—	nCK	
Exit active power-down mode to read command (slow exit, lower power)	t_{XARDS}	8 – AL	—	7 – AL	—	nCK	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	2	—	nCK	
Exit self-refresh to a non-read command	t_{XSNR}	t_{RFC} +10	—	t_{RFC} +10	—	ns	34)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	nCK	
Write command to DQS associated clock edges	WL	RL – 1		RL–1		nCK	

1) V_{DDQ} = 1.8 V ± 0.1V; V_{DD} = 1.8 V ± 0.1 V.
2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
3) Timings are guaranteed with CK/$\overline{\text{CK}}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
4) The CK / $\overline{\text{CK}}$ input reference level (for timing reference to CK / $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross. The DQS / $\overline{\text{DQS}}$, RDQS / $\overline{\text{RDQS}}$, input reference level is the crosspoint when in differential strobe mode.
5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
6) The output timing reference voltage level is V_{TT}.
7) New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2–667 and DDR2–800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2–400 and

DDR2–533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.

8) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(6-10per)}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{ERR(6-10PER).MIN}$ = – 272 ps and $t_{ERR(6-10PER).MAX}$ = + 293 ps, then $t_{DQSCK.MIN(DERATED)}$ = $t_{DQSCK.MIN}$ – $t_{ERR(6-10PER).MAX}$ = – 400 ps – 293 ps = – 693 ps and $t_{DQSCK.MAX(DERATED)}$ = $t_{DQSCK.MAX}$ – $t_{ERR(6-10PER).MIN}$ = 400 ps + 272 ps = + 672 ps. Similarly, $t_{LZ.DQ}$ for DDR2–667 derates to $t_{LZ.DQ.MIN(DERATED)}$ = - 900 ps – 293 ps = – 1193 ps and $t_{LZ.DQ.MAX(DERATED)}$ = 450 ps + 272 ps = + 722 ps. (Caution on the MIN/MAX usage!)
9) Input clock jitter spec parameter. The jitter specified is a random jitter meeting a Gaussian distribution.
10) These parameters are specified per their average values.
11) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.
12) DAL = WR + RU{t_{RP}(ns) / t_{CK}(ns)}, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For t_{RP}, if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period. Example: For DDR2–533 at t_{CK} = 3.75 ns with t_{WR} programmed to 4 clocks. t_{DAL} = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.
13) $t_{DAL.nCK}$ = WR [nCK] + $t_{nRP.nCK}$ = WR + RU{t_{RP} [ps] / $t_{CK.AVG}$[ps] }, where WR is the value programmed in the EMR.
14) Input waveform timing t_{DH} with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{IH.DC}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{IL.DC}$ level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{IL.DC.MAX}$ and $V_{IH.DC.MIN}$. See **Figure 4**.
15) t_{DQSQ}: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.
16) These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{\text{DQS}}$) crossing to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
17) Input waveform timing t_{DS} with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{IH.AC}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL.AC}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{il(DC)MAX}$ and $V_{ih(DC)MIN}$. See **Figure 4**.
18) If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
19) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS / $\overline{\text{DQS}}$) crossing.
20) t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for t_{QH} calculation is determined by the following equation; t_{HP} = MIN ($t_{CH.ABS}$, $t_{CL.ABS}$), where, $t_{CH.ABS}$ is the minimum of the actual instantaneous clock high time; $t_{CL.ABS}$ is the minimum of the actual instantaneous clock low time.
21) t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}) .
22) input waveform timing is referenced from the input signal crossing at the $V_{IL.DC}$ level for a rising signal and $V_{IH.DC}$ for a falling signal applied to the device under test. See **Figure 5**.
23) Input waveform timing is referenced from the input signal crossing at the $V_{IH.AC}$ level for a rising signal and $V_{IL.AC}$ for a falling signal applied to the device under test. See **Figure 5**.
24) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
25) t_{QH} = t_{HP} – t_{QHS}, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.} Examples: 1) If the system provides t_{HP} of 1315 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 975 ps minimum. 2) If the system provides t_{HP} of 1420 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 1080 ps minimum.
26) t_{QHS} accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.
27) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
28) 0 °C≤ T_{CASE} ≤ 85 °C.
29) 85 °C < T_{CASE} ≤ 95 °C.

30) A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 x t_{REFI}.
31) t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). **Figure 3** shows a method to calculate these points when the device is no longer driving (t_{RPST}), or begins driving (t_{RPRE}) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
32) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.PER}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.PER.MIN}$ = – 72 ps and $t_{JIT.PER.MAX}$ = + 93 ps, then $t_{RPRE.MIN(DERATED)} = t_{RPRE.MIN} + t_{JIT.PER.MIN}$ = 0.9 x $t_{CK.AVG}$ – 72 ps = + 2178 ps and $t_{RPRE.MAX(DERATED)} = t_{RPRE.MAX} + t_{JIT.PER.MAX}$ = 1.1 x $t_{CK.AVG}$ + 93 ps = + 2843 ps. (Caution on the MIN/MAX usage!).
33) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.DUTY}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.DUTY.MIN}$ = – 72 ps and $t_{JIT.DUTY.MAX}$ = + 93 ps, then $t_{RPST.MIN(DERATED)} = t_{RPST.MIN} + t_{JIT.DUTY.MIN}$ = 0.4 x $t_{CK.AVG}$ – 72 ps = + 928 ps and $t_{RPST.MAX(DERATED)} = t_{RPST.MAX} + t_{JIT.DUTY.MAX}$ = 0.6 x $t_{CK.AVG}$ + 93 ps = + 1592 ps. (Caution on the MIN/MAX usage!).
34) For these parameters, the DDR2 SDRAM device is characterized and verified to support t_{nPARAM} = RU{t_{PARAM} / $t_{CK.AVG}$}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support t_{nRP} = RU{t_{RP} / $t_{CK.AVG}$}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2–667 5–5–5, of which t_{RP} = 15 ns, the device will support t_{nRP} = RU{t_{RP} / $t_{CK.AVG}$} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm + 5 is valid even if (Tm + 5 - Tm) is less than 15 ns due to input clock jitter.
35) t_{WTR} is at lease two clocks (2 x t_{CK}) independent of operation frequency.
36) This timing parameter is relaxed than Industry Standard

FIGURE 3
Method for Calculating Transitions and Endpoint

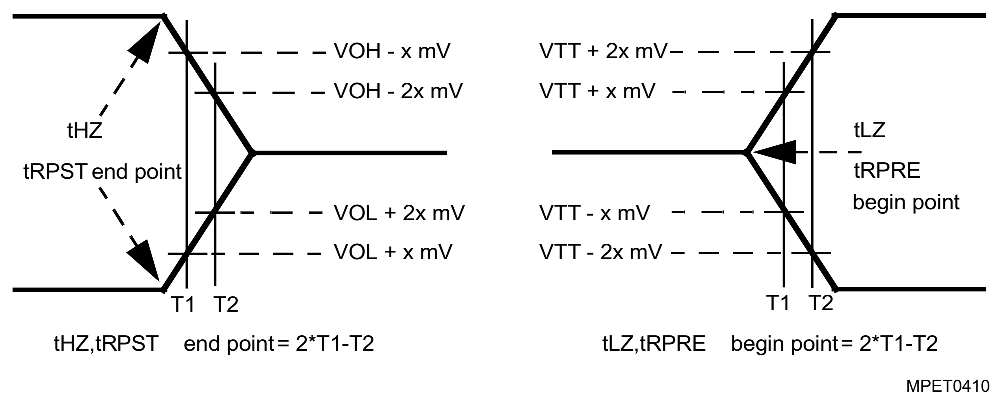


FIGURE 4
Differential Input Waveform Timing t_{DS} and t_{DH}

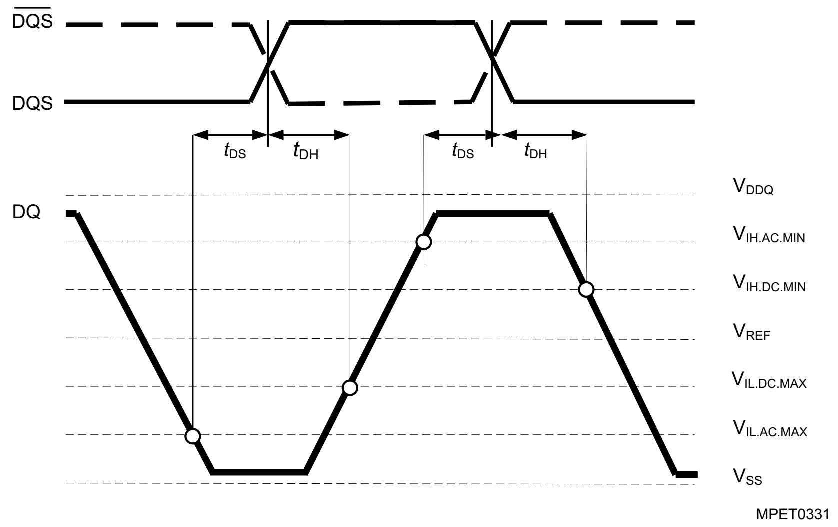
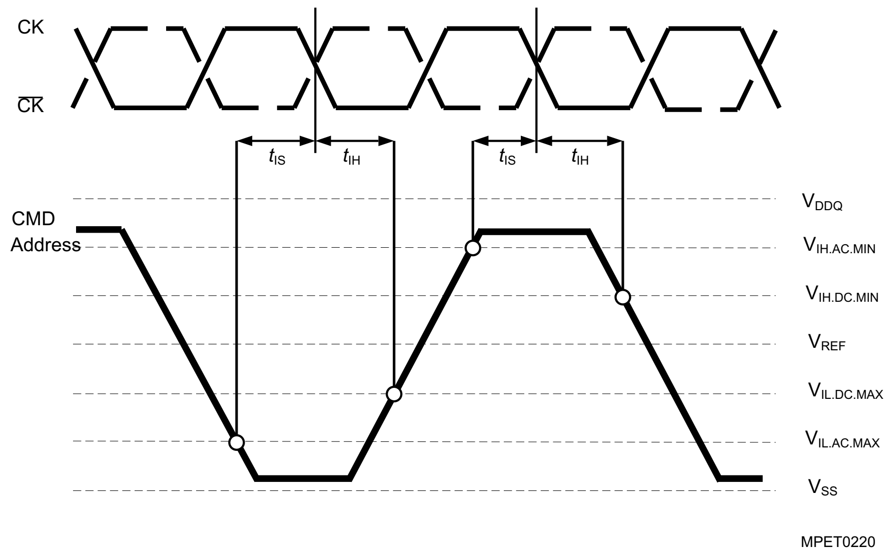


FIGURE 5
Differential Input Waveform Timing t_{IS} and t_{IH}



3.5 ODT AC Electrical Characteristics

This chapter describes the ODT AC electrical characteristics.

TABLE 15
ODT AC Characteristics and Operating Conditions for DDR2-667 , DDR2-800

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	n_{CK}	1)
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7 ns	ns	1)2)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	1)
t_{AOFD}	ODT turn-off delay	2.5	2.5	n_{CK}	1)
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	1)3)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	1)
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	n_{CK}	1)
t_{AXPD}	ODT Power Down Exit Latency	8	—	n_{CK}	1)

1) New units, "$t_{CK.AVG}$" and "n_{CK}", are introduced in DDR2-667 and DDR2-800 Unit "$t_{CK.AVG}$" represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit "n_{CK}" represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, "t_{CK}" is used for both concepts. Example: t_{XP} = 2 [n_{CK}] means; if Power Down exit is registered at T_m, an Active command may be registered at T_m + 2, even if (T_m + 2 - T_m) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.

2) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted differently per speed bin. For DDR2-667/800 t_{AOND} is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

3) ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-667/800, if $t_{CK(avg)}$ = 3 ns is assumed, t_{AOFD} is 1.5 ns (= 0.5 x 3 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

3.6 I_{DD} Specifications and Conditions

List of tables defining I_{DD} Specifications and Conditions.

TABLE 16
I_{DD} Measurement Conditions

Parameter	Symbol	Note[1)2)3)4)5)]
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}	
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = CL_{MIN}; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}	6)
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD2N}	
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}	
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}	
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$	
Operating Current - Burst Read All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CKMIN}$; $t_{RAS} = t_{RASMAX}$; $t_{RP} = t_{RPMIN}$; CKE is HIGH, CS is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; I_{OUT} = 0mA.	I_{DD4R}	6)
Operating Current - Burst Write All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}	
Burst Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}	
Distributed Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}	

Parameter	Symbol	Note[1)2)3)4)5)]
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{\text{CK}}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}	
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}	6)

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
3) Definitions for I_{DD} see **Table 17**
4) For two rank modules: All active current measurements in the same I_{DD} current mode. The other rank is in I_{DD2P} Precharge Power-Down Mode.
5) For details and notes see the relevant Qimonda component data sheet.
6) I_{DD1}, I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled (I_{OUT} = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

TABLE 17
Definitions for I_{DD}

Parameter	Description
LOW	$V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	Inputs are stable at a HIGH or LOW level.
FLOATING	Inputs are $V_{REF} = V_{DDQ}/2$
SWITCHING	Inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes.

TABLE 18
I_{DD} Specification for HYS[64/72]T512020EU–[25F/2.5/3S]–A

Product Type	HYS64T512020EU–25F–A	HYS72T512020EU–25F–A	HYS64T512020EU–2.5–A	HYS72T512020EU–2.5–A	HYS64T512020EU–3S–A	HYS72T512020EU–3S–A	Units	Note[1)2)]
Organization	4 GB	4 GB	4 GB	4 GB	4 GB	4 GB		
	×64	×72	×64	×72	×64	×72		
	2 Ranks	2 Ranks	2 Ranks	2 Ranks	2 Ranks	2 Ranks		
	–25F	–25F	–2.5	–2.5	–3S	–3S		
I_{DD0}	824	927	824	927	776	873	mA	3)
I_{DD1}	872	981	872	981	832	936	mA	3)
I_{DD2N}	1008	1134	1008	1134	928	1044	mA	4)
I_{DD2P}	256	288	256	288	256	288	mA	4)
I_{DD2Q}	976	1098	976	1098	880	990	mA	4)
I_{DD3N}	1104	1242	1104	1242	1008	1134	mA	4)
$I_{DD3P\_0\ (fast)}$	560	630	560	630	528	594	mA	4)5)
$I_{DD3P\_1\ (slow)}$	288	324	288	324	288	324	mA	4)6)
I_{DD4R}	1328	1494	1328	1494	1216	1368	mA	3)
I_{DD4W}	1448	1629	1448	1629	1328	1494	mA	3)
I_{DD5B}	1976	2223	1976	2223	1936	2178	mA	3)
I_{DD5D}	320	360	320	360	320	360	mA	4)7)
I_{DD6}	256	288	256	288	256	288	mA	4)7)
I_{DD7}	1872	2106	1872	2106	1728	1944	mA	3)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled.
2) $I_{DDX\ (rank)}$ = Number of components x $I_{DDX\ (component)}$
3) $I_{DDX} = I_{DDX\ (rank)} + I_{DD2P\ (rank)}$
4) $I_{DDX} = 2 \times I_{DDX\ (rank)}$
5) Fast: MRS(12)=0
6) Slow: MRS(12)=1
7) I_{DD5D} and I_{DD6} values are for $0°C \leq T_{Case} \leq 85°C$

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

TABLE 19
HYS[64/72]T512020EU-[25F/2.5]-A

Product Type		HYS64T512020EU–25F–A	HYS72T512020EU–25F–A	HYS64T512020EU–2.5–A	HYS72T512020EU–2.5–A
Organization		4 GByte	4 GByte	4 GByte	4 GByte
		×64	×72	×64	×72
		2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2–6400U–555	PC2–6400E–555	PC2–6400U–666	PC2–6400E–666
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08
3	Number of Row Addresses	0F	0F	0F	0F
4	Number of Column Addresses	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	61	61	61	61
6	Data Width	40	48	40	48
7	Not used	00	00	00	00
8	Interface Voltage Level	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	25	25	25	25
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	40	40	40	40
11	Error Correction Support (non-ECC, ECC)	00	02	00	02
12	Refresh Rate and Type	82	82	82	82

Product Type		**HYS64T512020EU–25F–A**	**HYS72T512020EU–25F–A**	**HYS64T512020EU–2.5–A**	**HYS72T512020EU–2.5–A**
Organization		**4 GByte**	**4 GByte**	**4 GByte**	**4 GByte**
		×64	**×72**	**×64**	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–555**	**PC2–6400E–555**	**PC2–6400U–666**	**PC2–6400E–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
13	Primary SDRAM Width	08	08	08	08
14	Error Checking SDRAM Width	00	08	00	08
15	Not used	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	08	08	08	08
18	Supported CAS Latencies	70	70	70	70
19	DIMM Mechanical Characteristics	01	01	01	01
20	DIMM Type Information	02	02	02	02
21	DIMM Attributes	00	00	00	00
22	Component Attributes	07	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	25	25	30	30
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	40	40	45	45
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	3D	3D	3D	3D
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	50	50	50	50
27	$t_{RP.MIN}$ [ns]	32	32	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	32	32	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D
31	Module Density per Rank	02	02	02	02
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	17	17	17	17
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	25	25	25	25
34	$t_{DS.MIN}$ [ns]	05	05	05	05
35	$t_{DH.MIN}$ [ns]	12	12	12	12
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E

Product Type		HYS64T512020EU–25F–A	HYS72T512020EU–25F–A	HYS64T512020EU–2.5–A	HYS72T512020EU–2.5–A
Organization		**4 GByte**	**4 GByte**	**4 GByte**	**4 GByte**
		×64	**×72**	**×64**	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–555**	**PC2–6400E–555**	**PC2–6400U–666**	**PC2–6400E–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00
40	t_{RC} and t_{RFC} Extension	30	30	00	00
41	$t_{RC.MIN}$ [ns]	39	39	3C	3C
42	$t_{RFC.MIN}$ [ns]	C3	C3	C3	C3
43	$t_{CK.MAX}$ [ns]	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	14	14	14	14
45	$t_{QHS.MAX}$ [ns]	1E	1E	1E	1E
46	PLL Relock Time	0F	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	50	50	50	50
48	Psi(T-A) DRAM	60	60	60	60
49	ΔT_0 (DT0)	5F	5F	57	57
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	44	44	44	44
51	ΔT_{2P} (DT2P)	43	43	43	43
52	ΔT_{3N} (DT3N)	31	31	31	31
53	$\Delta T_{3P.fast}$ (DT3P fast)	49	49	49	49
54	$\Delta T_{3P.slow}$ (DT3P slow)	2F	2F	2F	2F
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	72	72	72	72
56	ΔT_{5B} (DT5B)	3A	3A	3A	3A
57	ΔT_7 (DT7)	43	43	41	41
58	Psi(ca) PLL	00	00	00	00
59	Psi(ca) REG	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00
62	SPD Revision	12	12	12	12

Product Type		**HYS64T512020EU–25F–A**	**HYS72T512020EU–25F–A**	**HYS64T512020EU–2.5–A**	**HYS72T512020EU–2.5–A**
Organization		**4 GByte**	**4 GByte**	**4 GByte**	**4 GByte**
		×64	**×72**	**×64**	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–555**	**PC2–6400E–555**	**PC2–6400U–666**	**PC2–6400E–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
63	Checksum of Bytes 0-62	67	79	54	66
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Product Type, Char 1	36	37	36	37
74	Product Type, Char 2	34	32	34	32
75	Product Type, Char 3	54	54	54	54
76	Product Type, Char 4	35	35	35	35
77	Product Type, Char 5	31	31	31	31
78	Product Type, Char 6	32	32	32	32
79	Product Type, Char 7	30	30	30	30
80	Product Type, Char 8	32	32	32	32
81	Product Type, Char 9	30	30	30	30
82	Product Type, Char 10	45	45	45	45
83	Product Type, Char 11	55	55	55	55
84	Product Type, Char 12	32	32	32	32
85	Product Type, Char 13	35	35	2E	2E
86	Product Type, Char 14	46	46	35	35
87	Product Type, Char 15	41	41	41	41

Product Type		HYS64T512020EU–25F–A	HYS72T512020EU–25F–A	HYS64T512020EU–2.5–A	HYS72T512020EU–2.5–A
Organization		**4 GByte**	**4 GByte**	**4 GByte**	**4 GByte**
		×64	**×72**	**×64**	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–6400U–555**	**PC2–6400E–555**	**PC2–6400U–666**	**PC2–6400E–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
88	Product Type, Char 16	20	20	20	20
89	Product Type, Char 17	20	20	20	20
90	Product Type, Char 18	20	20	20	20
91	Module Revision Code	0x	0x	0x	0x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00
128 - 255	Blank for customer use	FF	FF	FF	FF

TABLE 20
HYS[64/72]T512020EU-3S-A

Product Type		HYS64T512020EU–3S–A	HYS72T512020EU–3S–A
Organization		4 GByte	4 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2–5300U–555	PC2–5300E–555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0F	0F
4	Number of Column Addresses	0A	0A
5	DIMM Rank and Stacking Information	61	61
6	Data Width	40	48
7	Not used	00	00
8	Interface Voltage Level	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45
11	Error Correction Support (non-ECC, ECC)	00	02
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	08	08
14	Error Checking SDRAM Width	00	08
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	08	08
18	Supported CAS Latencies	38	38
19	DIMM Mechanical Characteristics	01	01
20	DIMM Type Information	02	02
21	DIMM Attributes	00	00
22	Component Attributes	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C

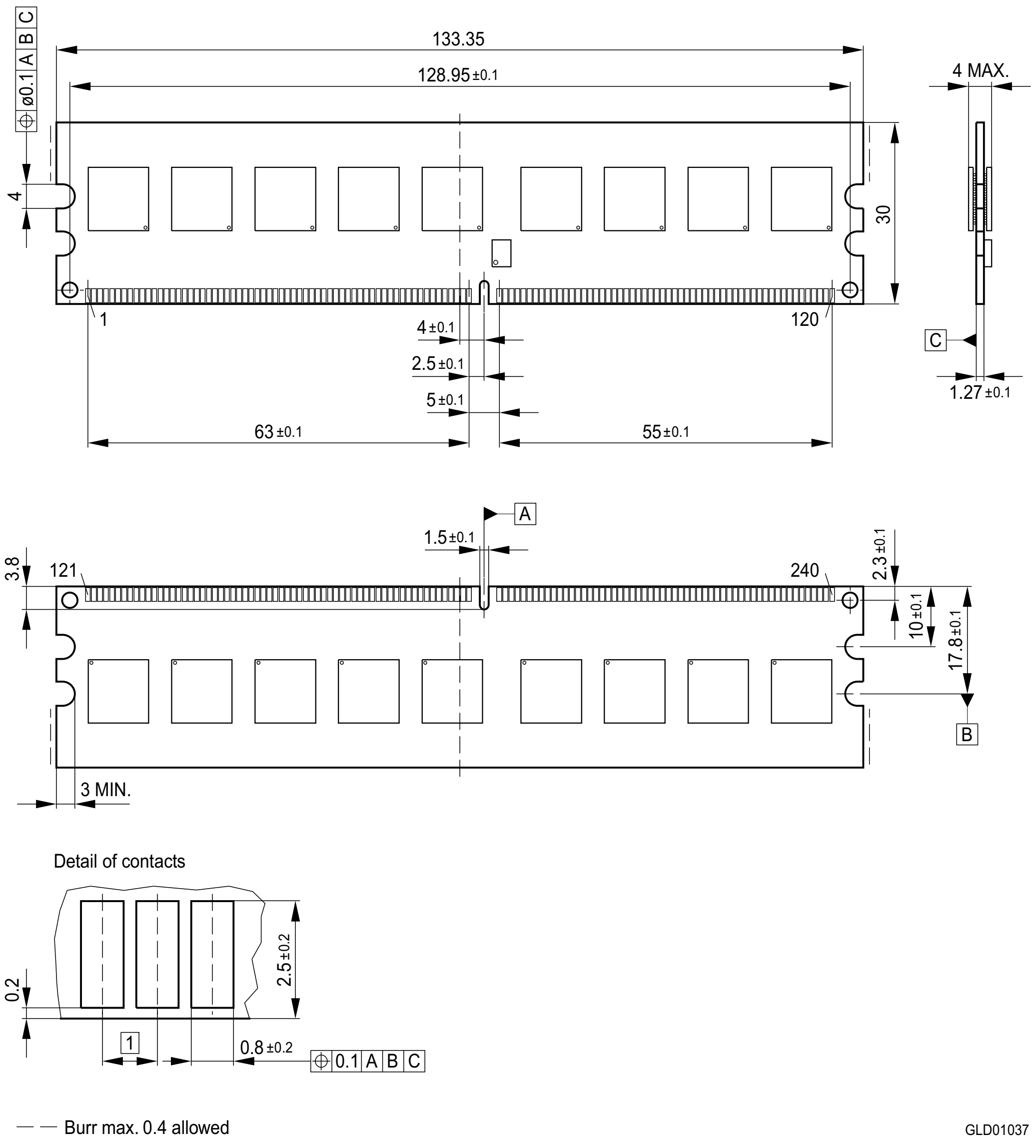
Product Type		**HYS64T512020EU–3S–A**	**HYS72T512020EU–3S–A**
Organization		**4 GByte**	**4 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–5300U–555**	**PC2–5300E–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**
30	$t_{RAS.MIN}$ [ns]	2D	2D
31	Module Density per Rank	02	02
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27
34	$t_{DS.MIN}$ [ns]	10	10
35	$t_{DH.MIN}$ [ns]	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E
39	Analysis Characteristics	00	00
40	t_{RC} and t_{RFC} Extension	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C
42	$t_{RFC.MIN}$ [ns]	C3	C3
43	$t_{CK.MAX}$ [ns]	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18
45	$t_{QHS.MAX}$ [ns]	22	22
46	PLL Relock Time	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	50	50
48	Psi(T-A) DRAM	60	60
49	ΔT_0 (DT0)	4B	4B
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	3B	3B
51	ΔT_{2P} (DT2P)	43	43
52	ΔT_{3N} (DT3N)	2B	2B
53	$\Delta T_{3P.fast}$ (DT3P fast)	42	42
54	$\Delta T_{3P.slow}$ (DT3P slow)	2F	2F
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	64	64
56	ΔT_{5B} (DT5B)	35	35
57	ΔT_7 (DT7)	35	35
58	Psi(ca) PLL	00	00
59	Psi(ca) REG	00	00
60	ΔT_{PLL} (DTPLL)	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00
62	SPD Revision	12	12

Product Type		HYS64T512020EU–3S–A	HYS72T512020EU–3S–A
Organization		4 GByte	4 GByte
		×64	×72
		2 Ranks (×8)	2 Ranks (×8)
Label Code		PC2–5300U–555	PC2–5300E–555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX
63	Checksum of Bytes 0-62	49	5B
64	Manufacturer’s JEDEC ID Code (1)	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00
72	Module Manufacturer Location	xx	xx
73	Product Type, Char 1	36	37
74	Product Type, Char 2	34	32
75	Product Type, Char 3	54	54
76	Product Type, Char 4	35	35
77	Product Type, Char 5	31	31
78	Product Type, Char 6	32	32
79	Product Type, Char 7	30	30
80	Product Type, Char 8	32	32
81	Product Type, Char 9	30	30
82	Product Type, Char 10	45	45
83	Product Type, Char 11	55	55
84	Product Type, Char 12	33	33
85	Product Type, Char 13	53	53
86	Product Type, Char 14	41	41
87	Product Type, Char 15	20	20
88	Product Type, Char 16	20	20
89	Product Type, Char 17	20	20
90	Product Type, Char 18	20	20
91	Module Revision Code	0x	0x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95 - 98	Module Serial Number	xx	xx

Product Type		**HYS64T512020EU–3S–A**	**HYS72T512020EU–3S–A**
Organization		**4 GByte**	**4 GByte**
		×64	**×72**
		2 Ranks (×8)	**2 Ranks (×8)**
Label Code		**PC2–5300U–555**	**PC2–5300E–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**
99 - 127	Not used	00	00
128 - 255	Blank for customer use	FF	FF

5 Package Outlines

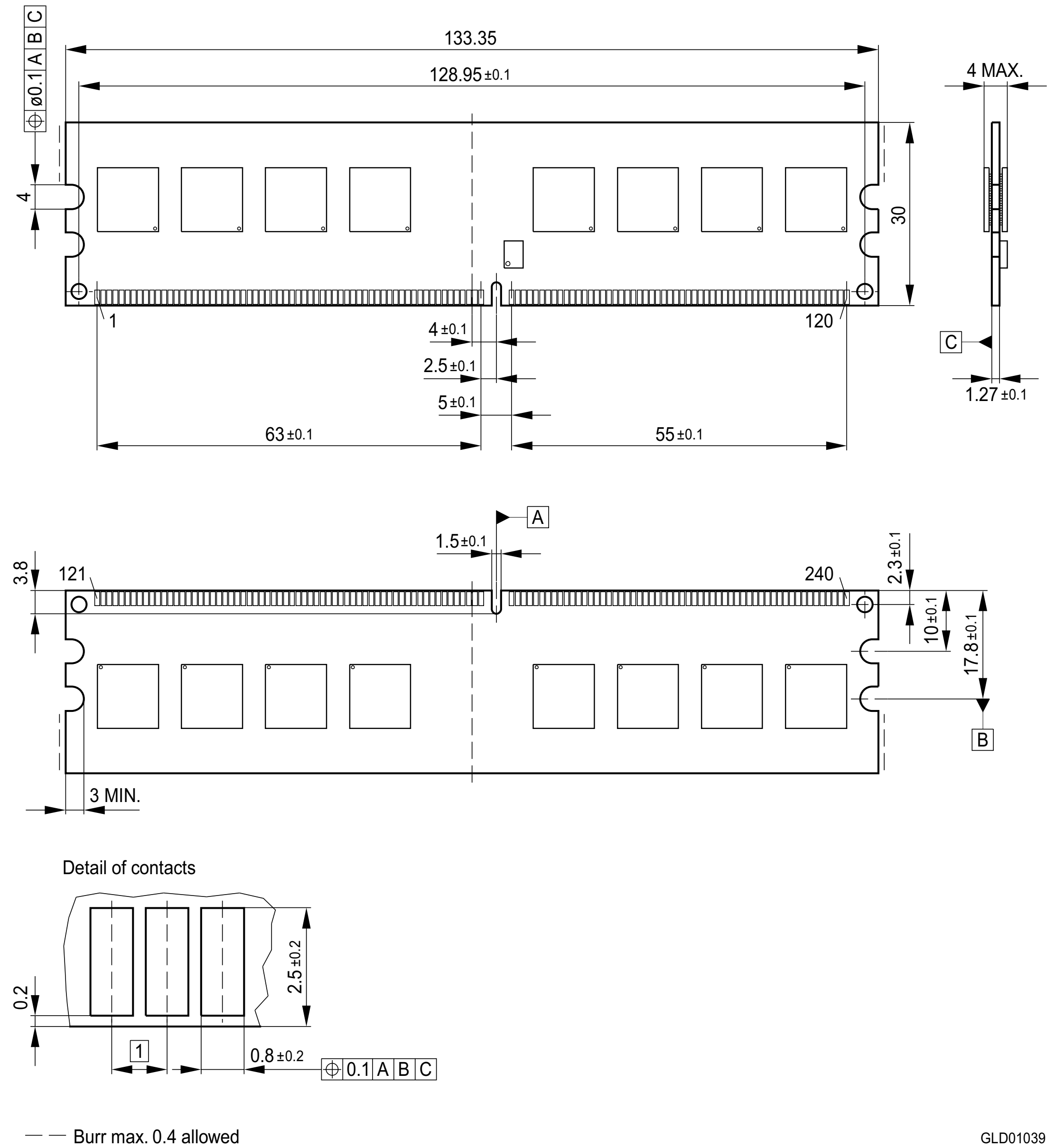
FIGURE 6
Package Outline L-DIM-240-107 Raw Card G



Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

FIGURE 7
Package Outline L-DIM-240-109 Raw Card E



Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

6 Product Type Nomenclature

Qimonda's nomenclature uses simple coding combined with some proprietary coding. **Table 21** provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 22** and for components in **Table 23**.

TABLE 21
Nomenclature Fields and Examples

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
Micro-DIMM	HYS	64	T	64/128	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512/1G	16		0	A	C	–5	

TABLE 22
DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	Qimonda Module Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
		F	**F**ully Buffered

Field	Description	Values	Coding
10	Speed Grade	–19F	PC2–8500 6–6–6
		–1.9	PC2–8500 7–7–7
		–25F	PC2–6400 5–5–5
		–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

TABLE 23
DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	Qimonda Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–19F	PC2–8500 6–6–6
		–1.9	PC2–8500 7–7–7
		–25F	PC2–6400 5–5–5
		–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3

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